What is Claimed is:

Sub A2

1. A method of operating a digital system having a processor and associated translation lookaside buffer (TLB), comprising the steps of:

executing a plurality of program tasks within the processor;

initiating a plurality of memory access requests in response to the plurality of program tasks;

caching a plurality of translated memory addresses in the TLB responsive to the plurality of memory access requests;

incorporating a task identification value with each translated memory address to identify which of the plurality of program tasks requested the respective translated memory address; and

locking or unlocking a portion of the plurality of translated memory address in the TLB in a manner that is qualified by the task identification value, such that only an entry of a selected program task in the plurality of translated memory addresses is affected.

2. The method according to Claim 1, wherein the step of locking or unlocking comprises locking or unlocking only and all of the plurality of translated addresses that have the selected task identification value.

3. The method of Claim 2, wherein the TLB has several levels, and wherein the step of locking or unlocking encompasses all of the several levels of the TLB.

4. The method according to Claim 3, further comprising the step of incorporating a second qualifier value with each translated memory address; and

wherein the step of locking or unlocking is qualified by both the task identification value and the second qualifier value.

Cont A2

5. The method of Claim 4, wherein the digital system has a plurality of processors and wherein the second qualifier value identifies which of the plurality of processor requested the respective translated memory address.

6. The method according to Claim 5, further comprising the step of replacing a selected victim translated memory address with a different translated memory address, wherein the victim translated memory address is selected only from a portion of the plurality of translated memory addresses in the TLB that is not locked.

7. The method according to Claim 6, further comprising the step of reserving a portion of the entry locations from being locked.

8. A digital system having a translation lookaside buffer (TLB), the TLB comprising:

storage circuitry with a plurality of entry locations for holding translated values, wherein each of the plurality of entry locations includes a first field for a translated value and a second field for an associated qualifier value;

a set of inputs for receiving a translation request;

a set of outputs for providing a translated value selected from the plurality of entry locations; and

control circuitry connected to the storage circuitry, wherein the control circuitry is responsive to an operation command to lock or unlocked selected ones of the plurality of entry locations which have a first qualifier value in the second field.

9 The digital system of Claim 8, wherein the digital system further comprises a second level TLB connected to the TLB, the second level TLB comprising:

second level storage circuitry with a plurality of entry locations for holding translated values, wherein each of the plurality of entry locations includes a first field for a translated value and a second field for an associated qualifier value; and

wherein the control circuitry is connected to the second level storage circuitry, the control circuitry being responsive to an operation command to lock or unlock selected ones of the plurality of entry locations in the second storage circuitry which have a first qualifier value in the second field, such that qualified entry locations in the TLB and in the second level TLB are locked or unlocked in response to a single operation command.

10. The digital system according to Claim 8, wherein each of the plurality of entry locations in the storage circuitry contain a third field for a second associated qualifier value, and

wherein the control circuitry is responsive to an operation command to lock or unlock selected ones of the plurality of entry locations which have both a specified task ID value in the second field and a specified resource ID value in the third field.

11. The digital system according to Claim 8, wherein the control circuitry comprises:

a shift register connected to the storage circuitry for selecting a next victim entry location; and

skip circuitry connected to the shift register and to the storage circuitry, the skip circuitry operable to cause the shift register to skip over locked entry locations.

12. The digital system according to Claim 8, wherein the control circuitry comprises reservation circuitry operable to reserve a portion of the entry locations from being locked.

13. The digital system according to Claim 8 being a personal digital assistant, further comprising:

a processor (CPU) connected to the TLB and thereby connected to access a memory circuit;

a display, connected to the CPU via a display adapter;

radio frequency (RF) circuitry connected to the CPU; and

an aerial connected to the RF circuitry.